REMARKS

Claims 1-90 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-8, 12-20, 24-31, 35-42, 46-53, 57-64, 68-75, 79-86, and 90 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn et al. (U.S. Pat. No. 6,463,570) and further in view of Sunter et al. (U.S. Pat. No. 6,204,694). This rejection is respectfully traversed.

With respect to claim 1, as best understood by Applicant, Dunn, either singly or in combination with Sunter, fails to show, teach, or suggest an apparatus for testing an integrated circuit comprising **a plurality of clocked storage elements interconnected by a plurality of signal paths**, the apparatus comprising an analysis circuit adapted to identify **one of the signal paths** as flawed based on the change of the duration to the second duration. Instead, Dunn appears to disclose identifying **faulty wafer regions**.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, the alleged combination fails to disclose the limitation of an analysis circuit adapted to identify **one**

of **the signal paths interconnecting a plurality of clocked storage elements as flawed** based on the change of the duration to the second duration.

The present invention is directed to testing clocked storage elements that are interconnected by signal paths. For example, "circuit 202 comprises a plurality of clocked storage elements such as flip-flops that are interconnected by a plurality of signal paths...Each clocked storage element comprises a clock input to receive a clock signal." (Paragraph [0028]). In other words, the signal paths in the limitation "an analysis circuit adapted to identify one of the signal paths as flawed" specifically refer to the **signal paths interconnecting the clocked storage elements** as indicated in claim 1, not silicon wafer regions. As shown in an exemplary embodiment in FIG. 2 of the present application, an analysis circuit 214 indicates one of the signal paths as flawed as described in Paragraph [0049].

The Examiner acknowledges that Sunter fails to disclose this limitation. Instead, the Examiner relies on Dunn to disclose an analysis circuit that identifies one of the signal paths as flawed. Applicant respectfully notes that Dunn still fails to make up for the deficiencies of Sunter and instead discloses identifying faulty wafer regions (i.e. layers).

For example,

> A ring oscillator is fabricated on each die constituting the integrated device being manufactured. As is well known in the art, the dice are formed on a wafer of semiconductor material, typically silicon, each wafer containing a plurality of integrated circuit dice. During wafer test, a scan of the frequency of the ring oscillator for each die under test is made across the wafer. **Deviations in the ring oscillator frequency from a preselected nominal value delimit regions of the wafer in which the salicidation or other process step is marginal**. (See Column 2, Lines 36-46; Emphasis added).

And,

> The resistances associated with the salicide layer 120 are affected by the quality of the formation of the layer, and a marginal fabrication step may give rise to an enhanced resistance being contributed by the corresponding portion of salicide layer 120. For example, if the portion of the salicide layer 120 over one or both of the STI edges 122 is thinned, the corresponding resistances, R.sub.2 and R.sub.2 ' may be increased over the nominal value of these resistances.
>
> **Such imperfections in the salicide layer** 120 can degrade performance of the integrated circuit device being fabricated. Moreover, process variations giving rise to marginal layer formation may be localized over portions of the wafer being manufactured. As previously discussed, present methods for verifying polysilicon integrity may be insensitive to these effects. (See Column 3, Lines 50-65; Emphasis added).

Dunn discloses that ring oscillators are used to detect salicide layer imperfections (See Column 3, Line 65 through Column 4, Line 2). Imperfections in a particular **salicide layer** result in a period change in an output signal of a corresponding ring oscillator. The salicide layers are not signal paths between clocked storage elements. As such, Applicant respectfully submits that Dunn fails to disclose identifying **one of the signal paths interconnecting a plurality of clocked storage elements as flawed** as claim 1 recites.

Further, claim 1 recites **changing the duration of m selected pulses to a second duration** and identifying one of the signal paths as flawed **based on the change of the duration** to the second duration. In contrast, Dunn discloses that **a change in period of the ring oscillators indicates** a flawed salicide layer. Claim 1 is directed to deliberately changing a specific pulse duration, and identifying a flawed signal path based on a failure **caused by** the changed duration. The alleged combination fails to disclose this structure.

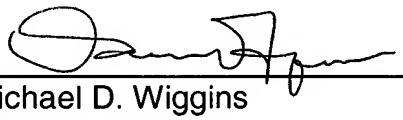
Applicant respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least similar reasons. The remaining independent claims, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: February 19, 2007

By: 

Michael D. Wiggins
Reg. No. 34,754
Damian M. Aquino
Reg. No. 54,964

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/DMA